

FIG. 1

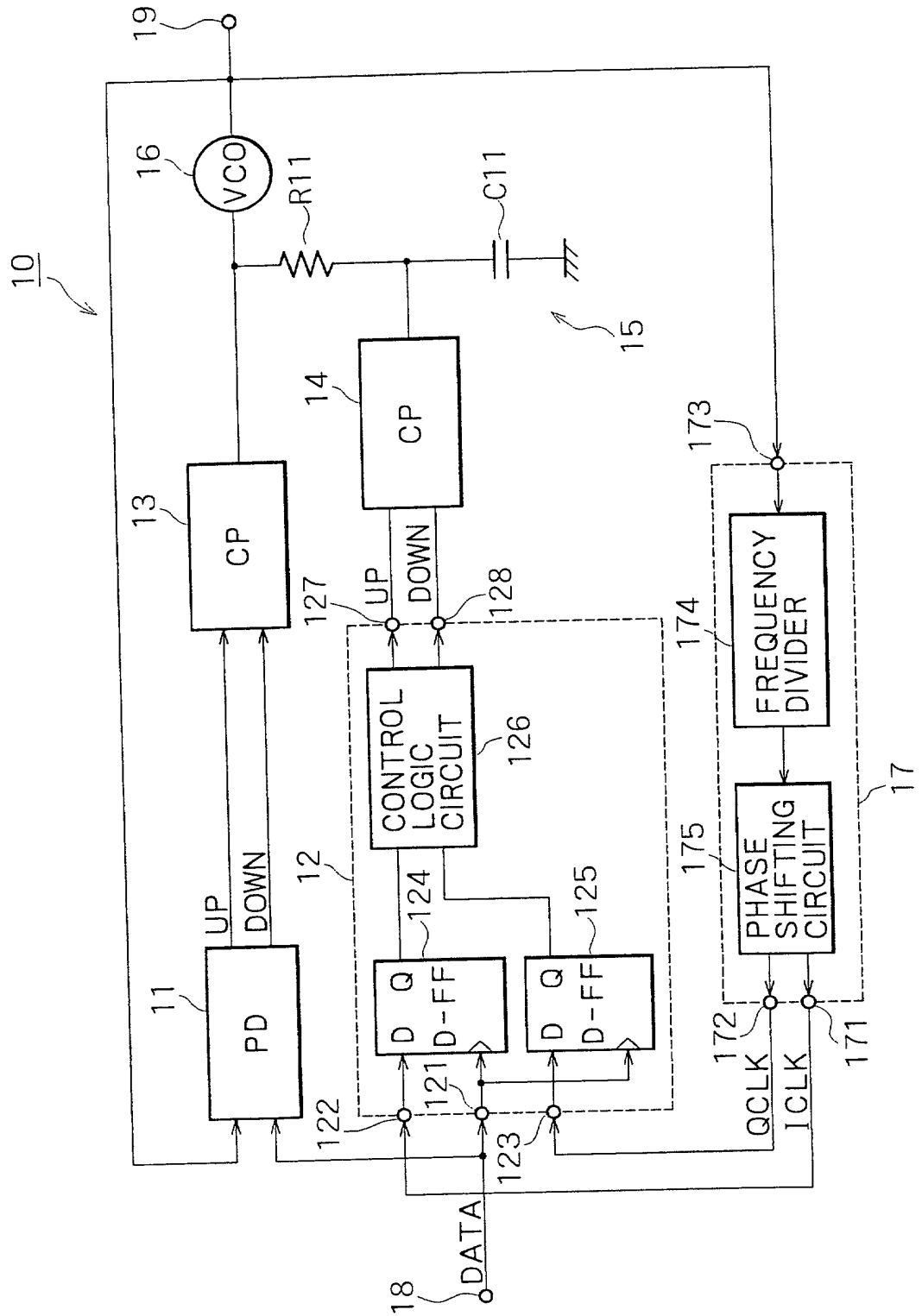


FIG. 2

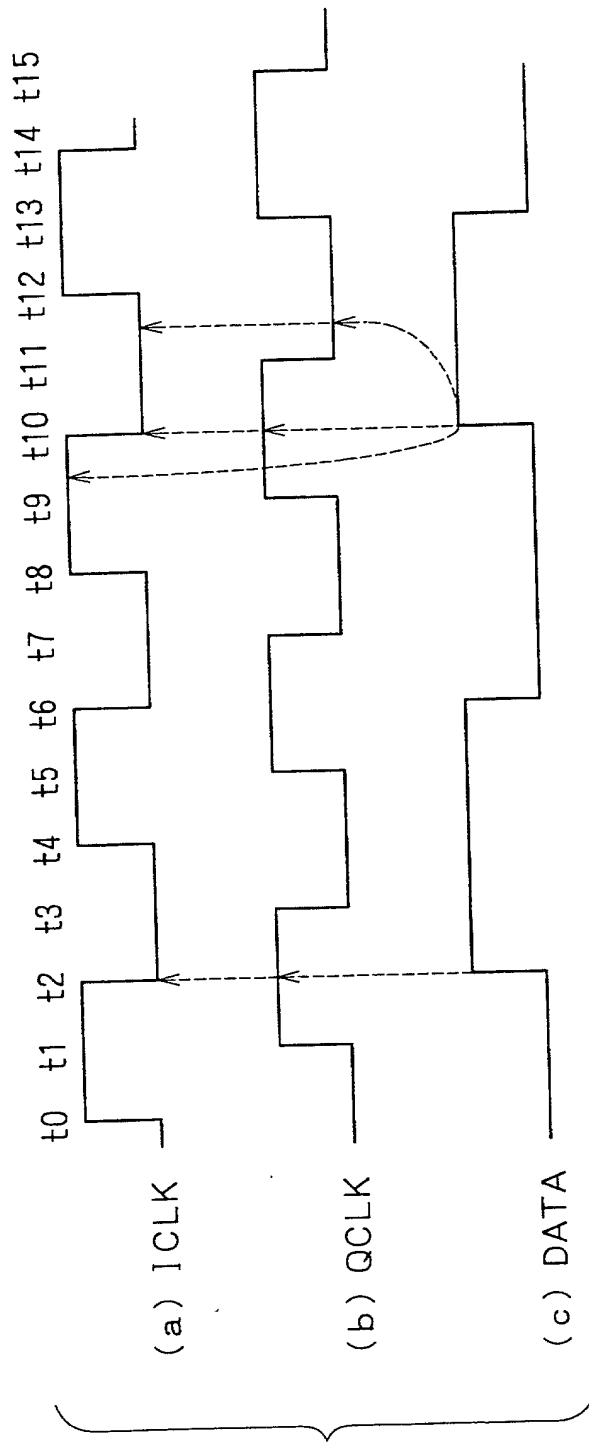


FIG. 3

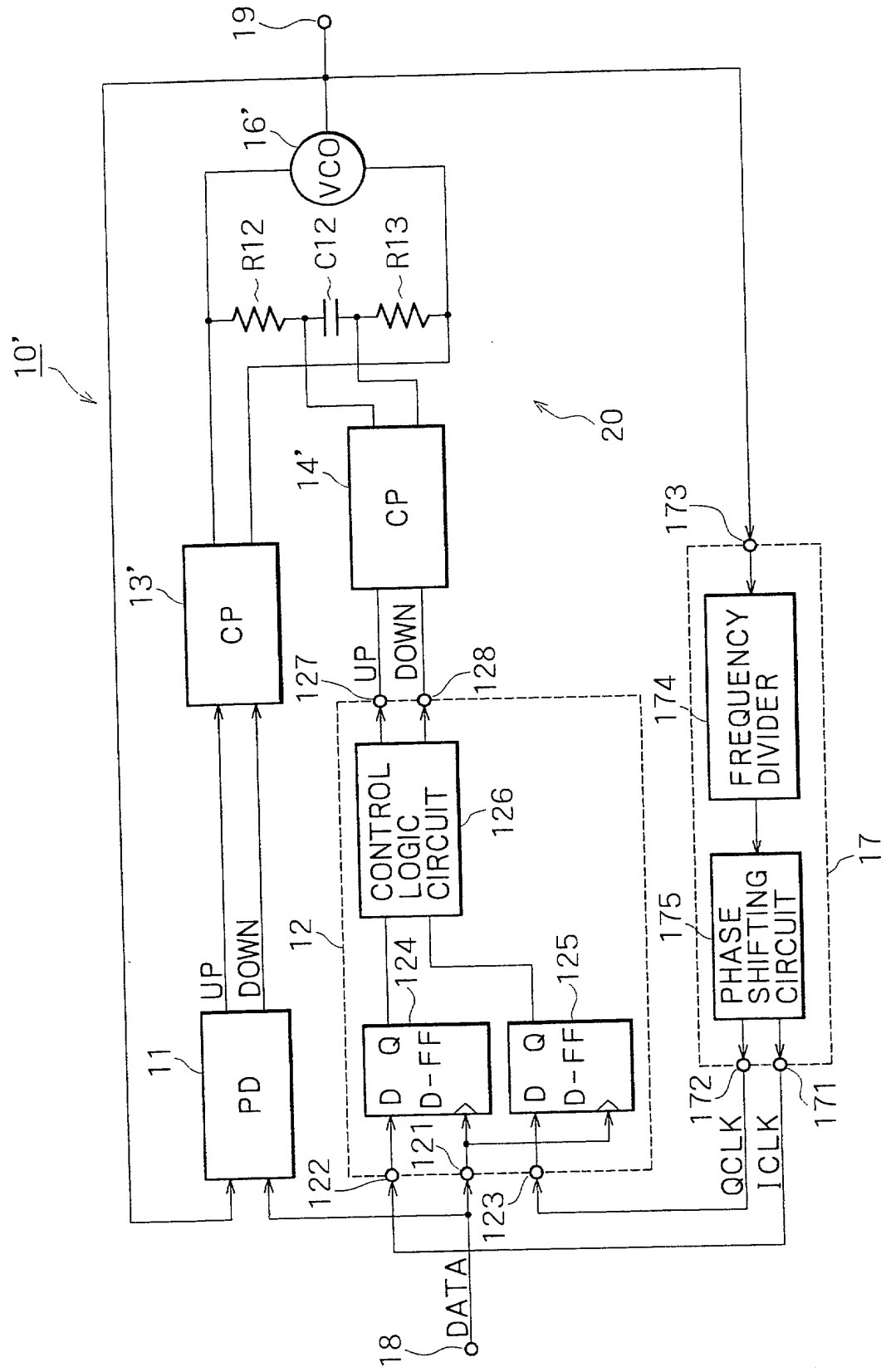


FIG. 4

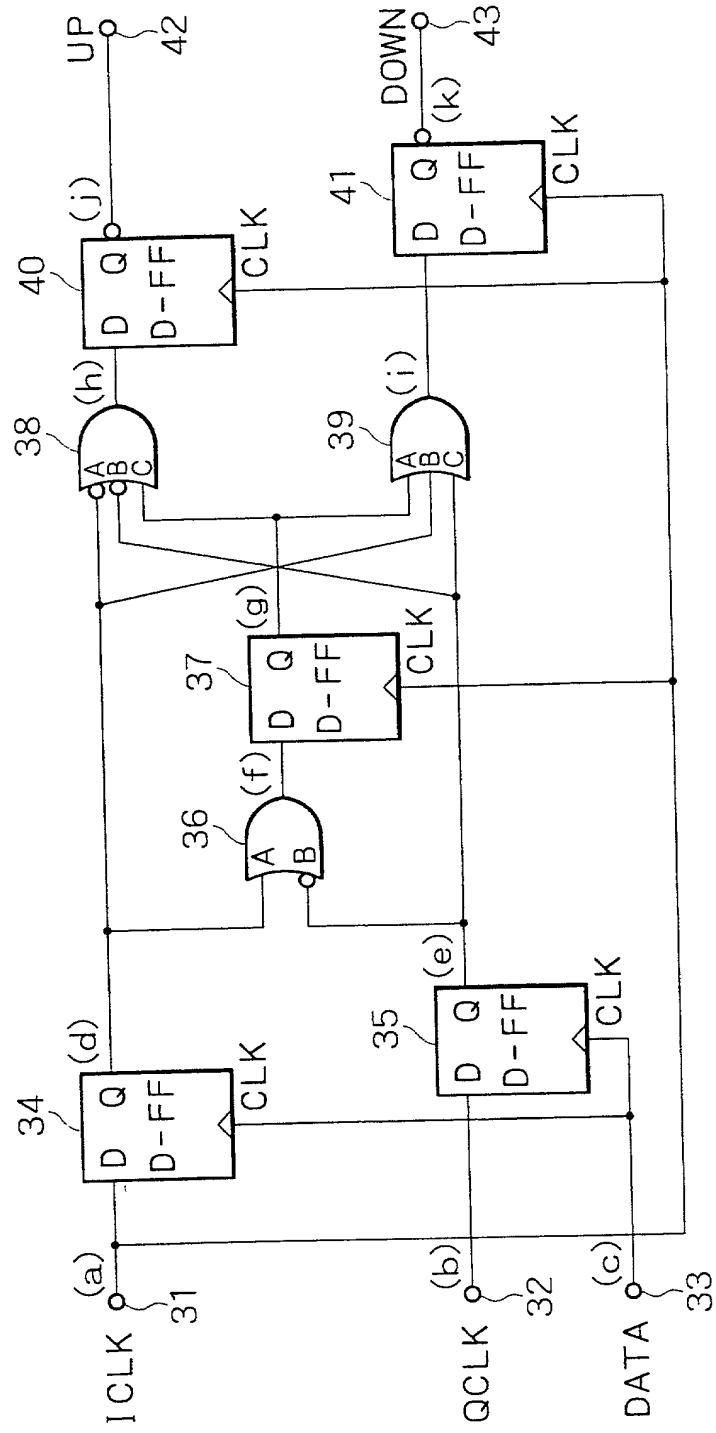


FIG. 5

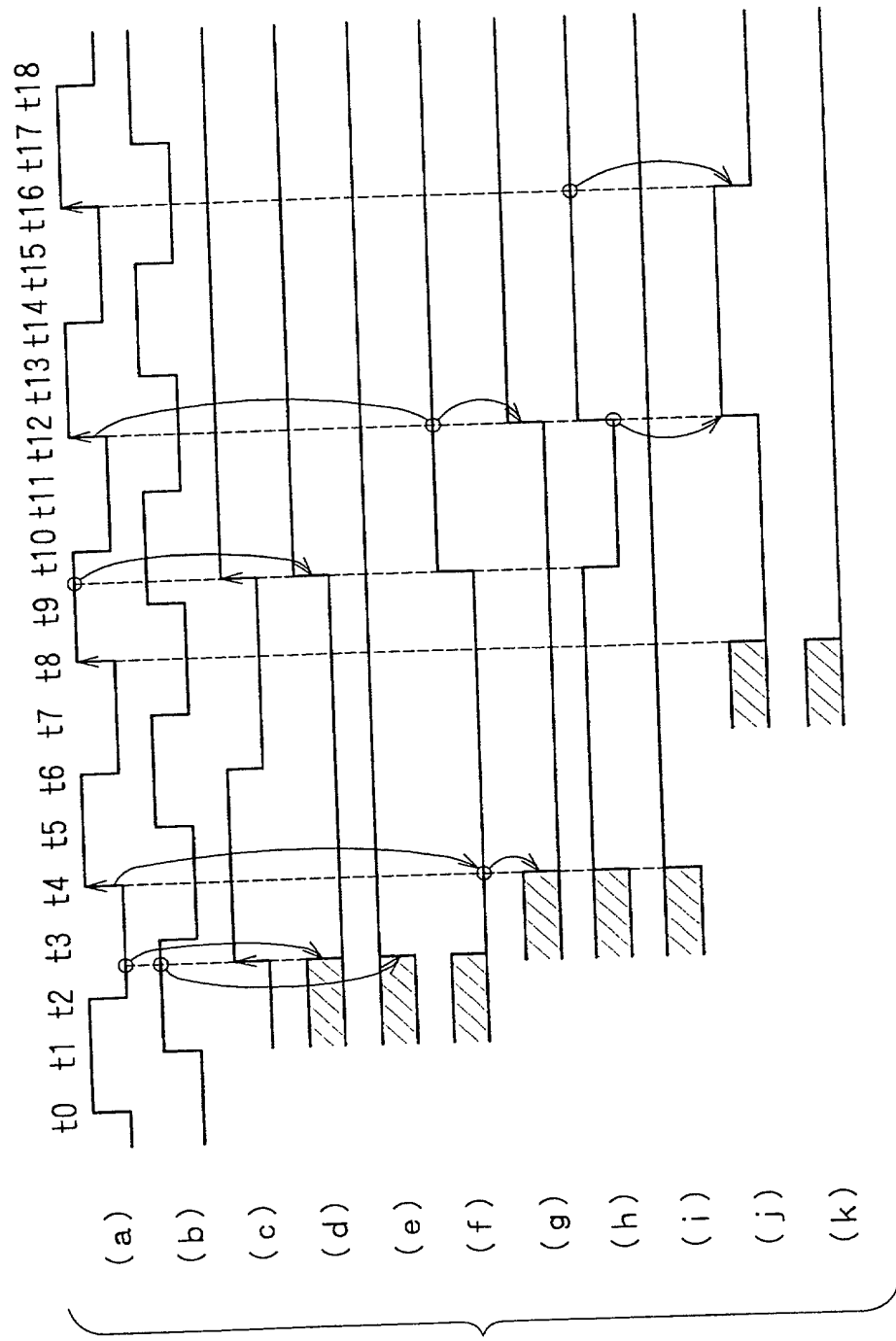


FIG. 6

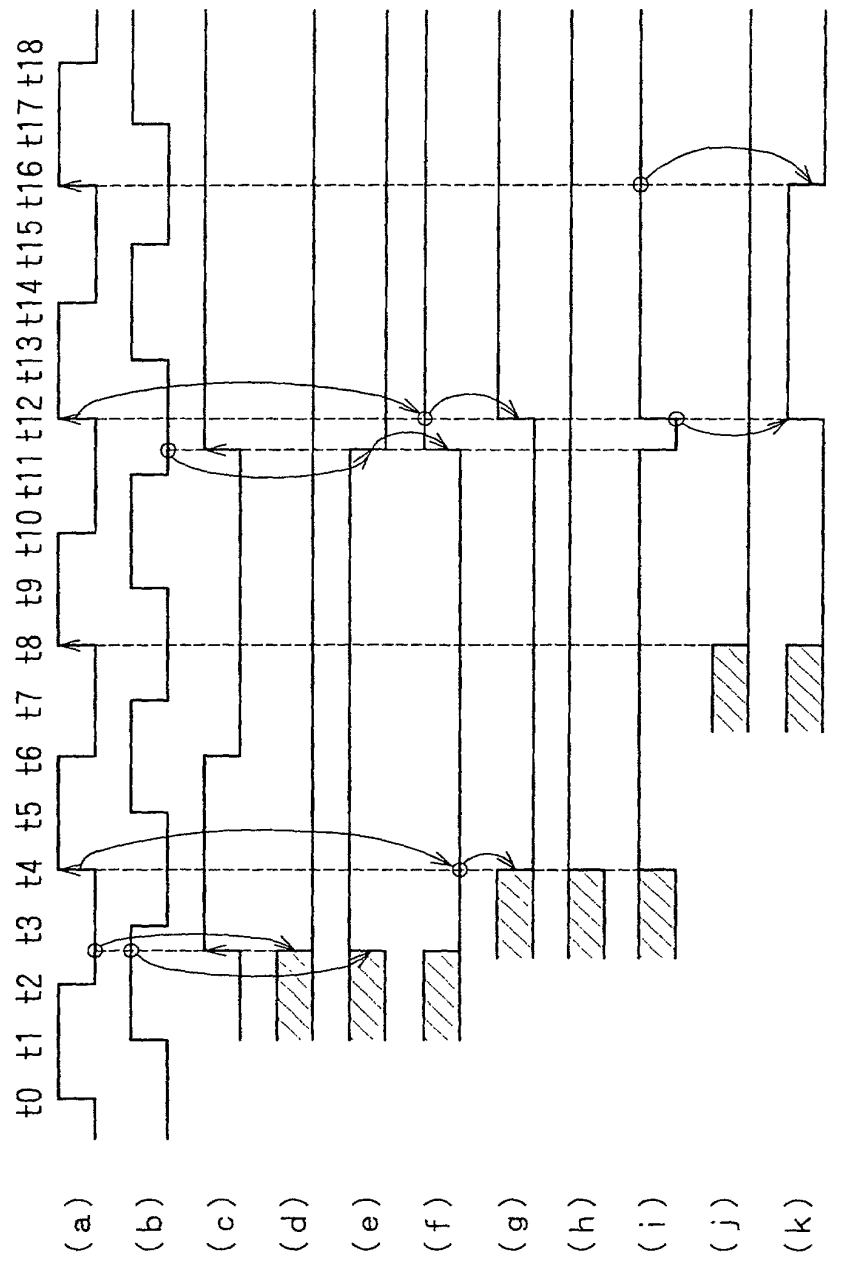


FIG. 7

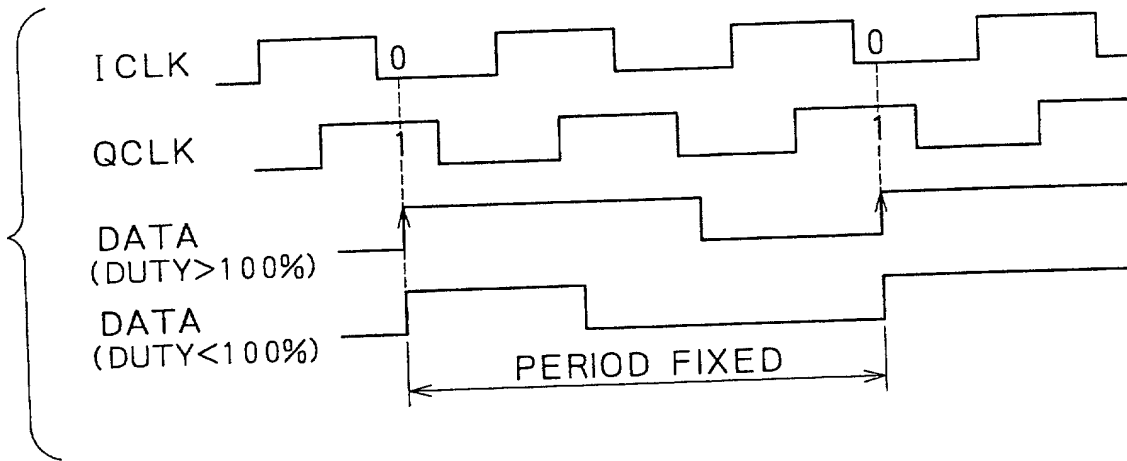
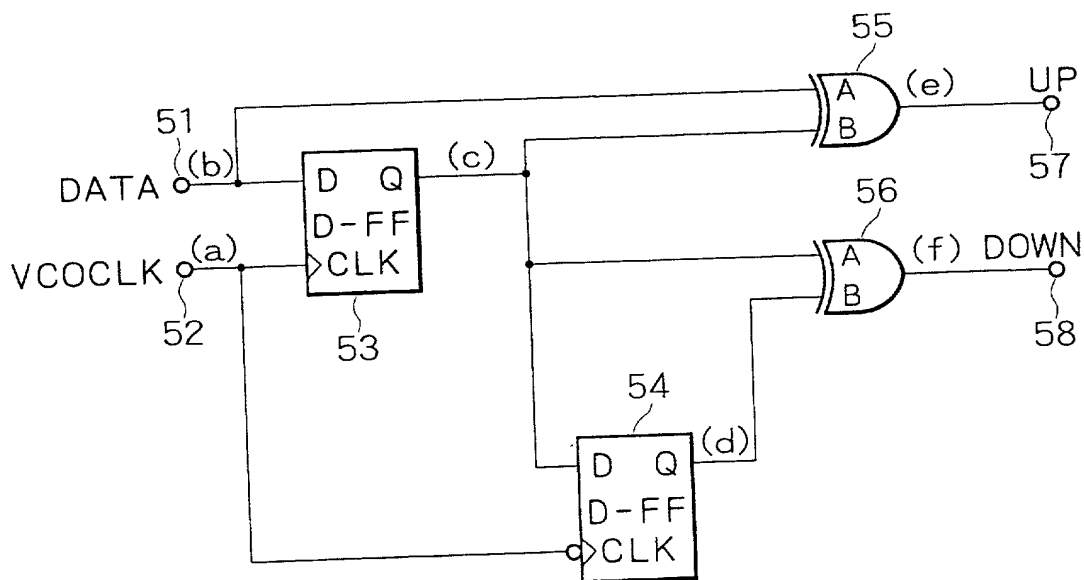


FIG. 8



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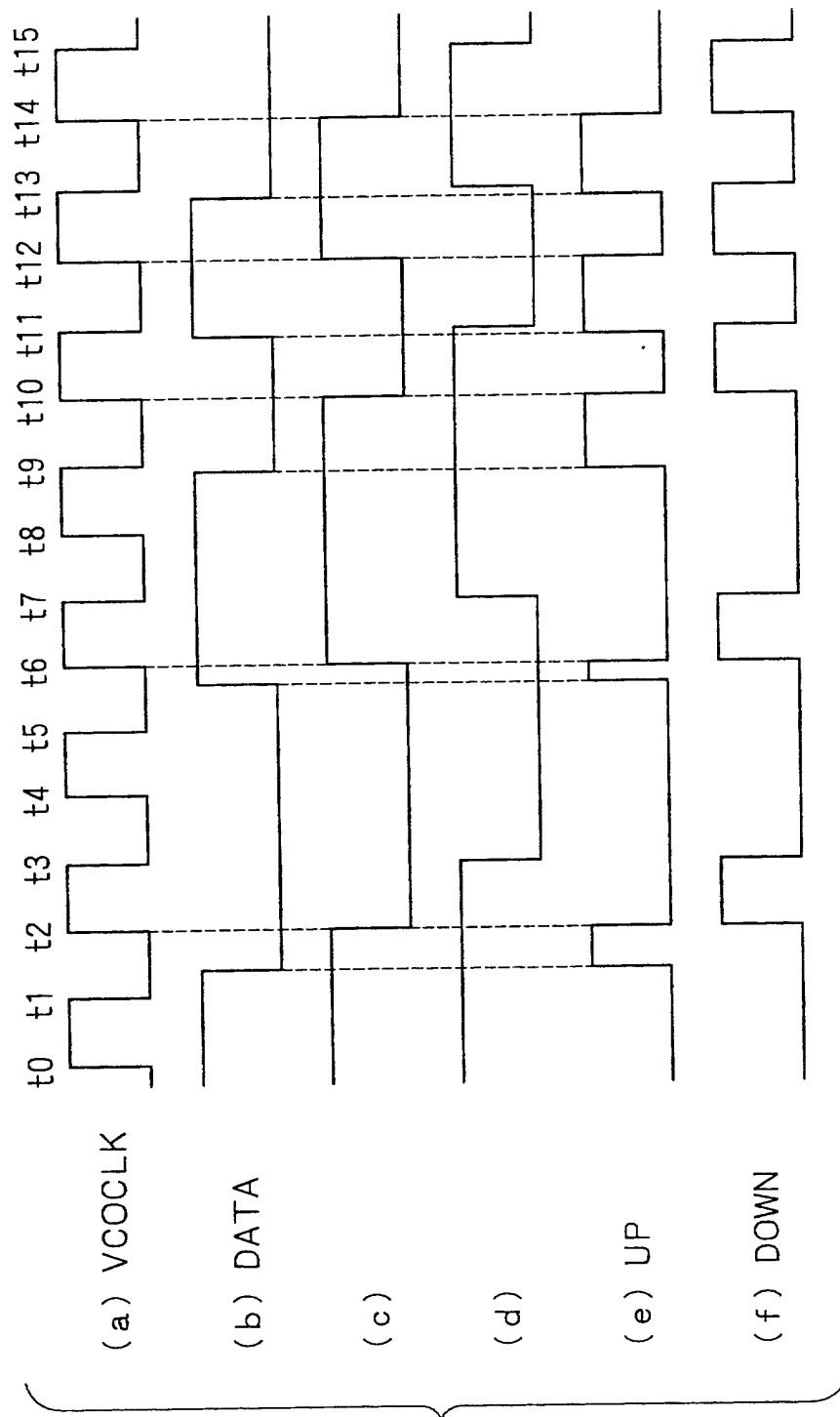


FIG. 10

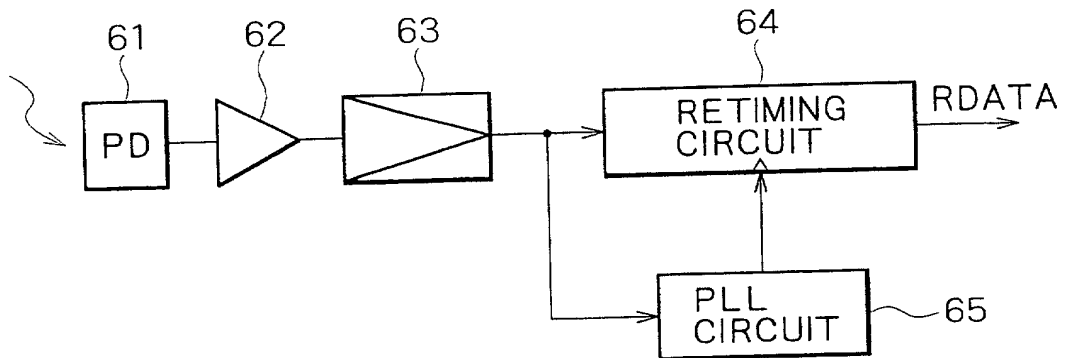


FIG. 11

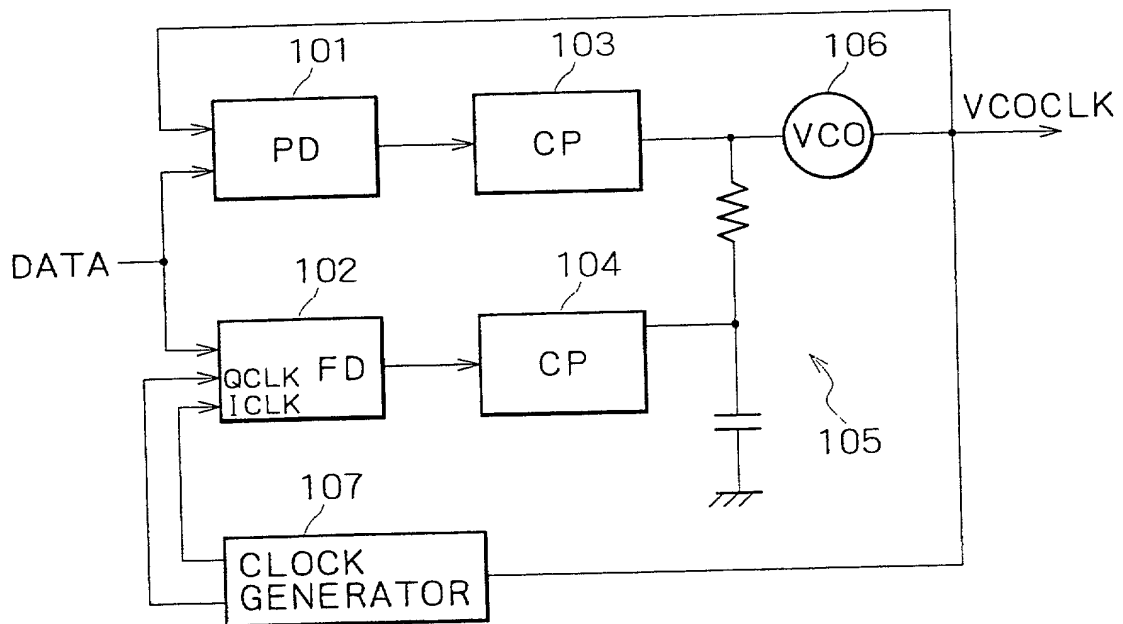
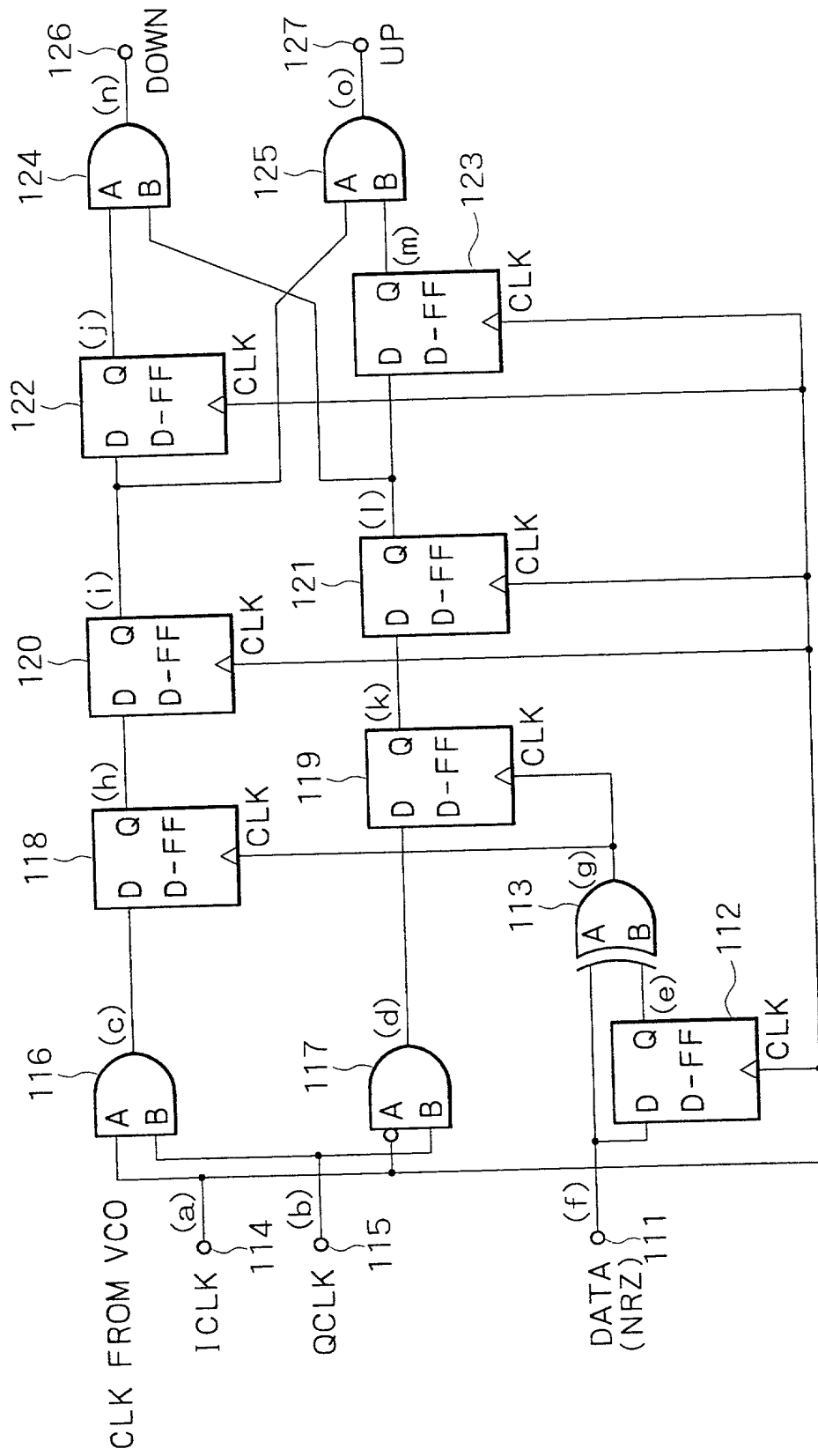


FIG. 12



ICLK: VCO OUTPUT CLK
QCLK: DELAYED BY 90° FROM ICLK

FIG. 13

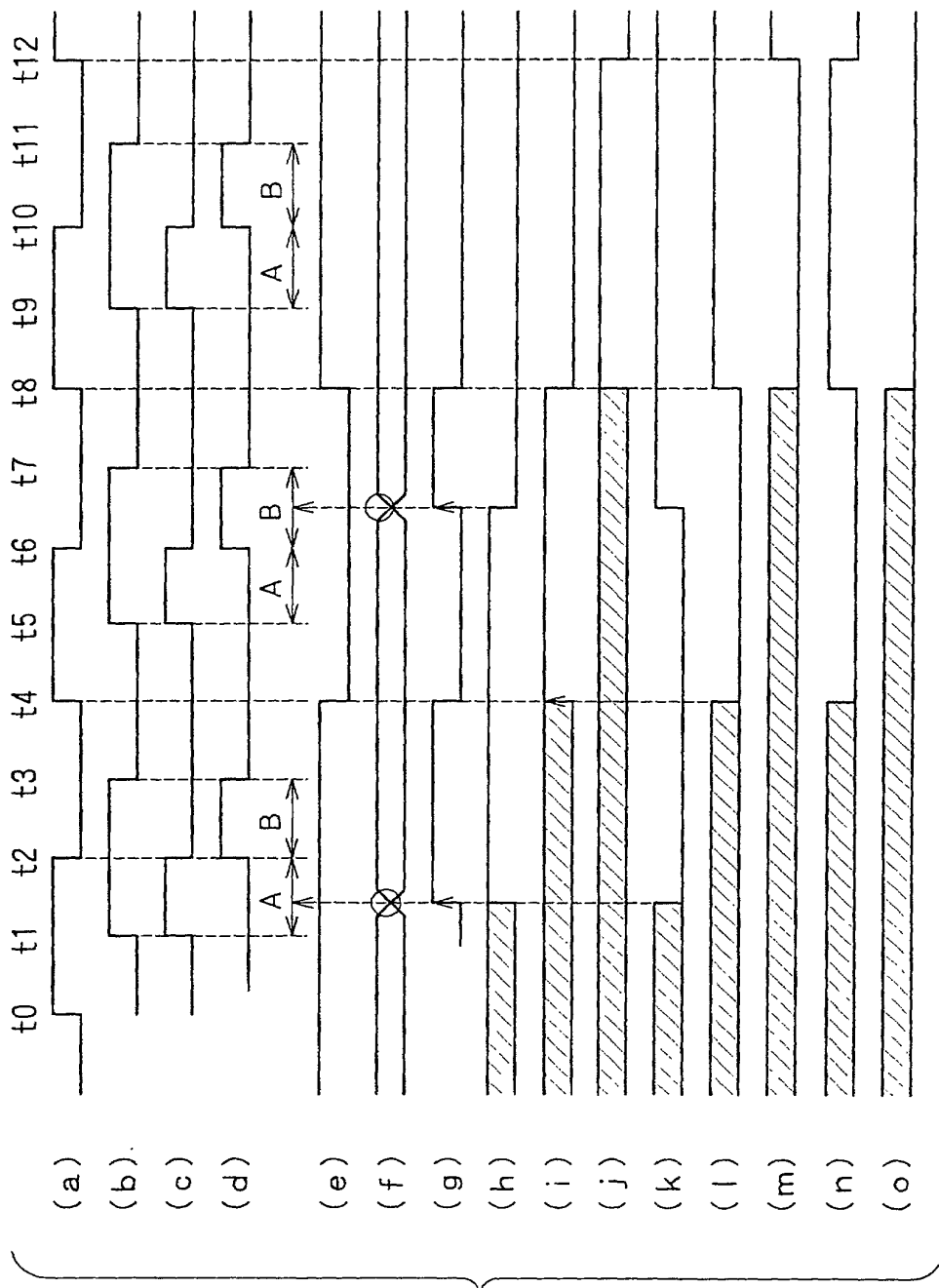


FIG. 14

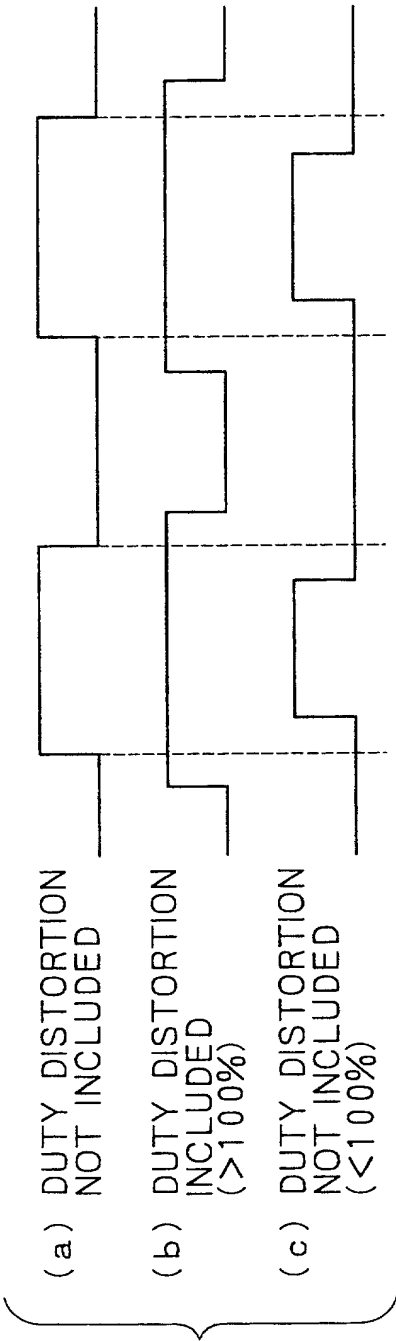


FIG. 15

